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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,382	07/28/2003	Graham Kirsch	501275.02	6524

7590 01/20/2006

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,382	KIRSCH, GRAHAM	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-38* is/are allowed.

6)☒ Claim(s) *1-12 and 39-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, and 5-7,43-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (patent No. 5,689,661).

3. Hayashi taught (claims 1,13) the invention as claimed including a data processing ("DP") system comprising: a logical array of processing elements logically arranged in a rectangular grid of logical rows and logical columns in which each processing element lies in only one logical row and one logical column (e.g., see fig. 6), the processing elements in the array being divided into four sub-arrays each including the processing elements in a respective quartile of the logical array (e.g., see col. 8, lines 57-col. 9, line 7)[four 8x8 subunits in the 16x16 array], each including processing elements in each of the sub-arrays being physically positioned in a folded arrangement in which the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical columns are physically interleaved with each other (e.g. see fig. 10 and col. 9, line 27-col. 10,line 8); and a system of conductors coupling the processing elements in each of the logical rows and columns of each other (e.g., see fig. 2,3a,3b,3c,3d,4a,4b,5a,5b,5c,6,8b,10).

4. As per claim 2, Hayashi taught the processing elements in each logical column are separated from each other by one processing elements (e.g., see fig. 6).

5. As per claim 3, Hayashi taught the processing elements in a logical row are separated from each other by three processing elements (e.g., see figs. 6, 3b, 4a, 5a, 5b, 5c, 10) [switches are positioned for providing connection between processing elements in a row that are separated by three processing elements].

6. As per claim 5, Hayashi taught the logical array of processing elements comprises upper and lower edge and wherein the processing elements in each of the subarrays are physically positioned so that the processing elements adjacent to the logical upper edge are physically positioned adjacent the processing elements adjacent the logical lower edge (e.g., see figs. 6,7).

7. As per claim 6, Hayashi taught the logical array is divided into upper and lower sections of processing elements separated from each other by a divide line, and wherein the processing elements in each of the sub-arrays are physically positioned so that the lowest processing elements in the logical upper section are adjacent the highest processing elements in the logical lower section on opposite sides of the divide line (e.g., see figs 6,7 and col. 8, line 57-col. 9, line 7)[when the array in figures 6 and 7 are divided as taught by Hayashi into subunits, the lowest processing elements in one subunit would be adjacent the upper processing elements in a lower adjacent subunit].

8. As per claim 7, Hayashi taught each sub-array is logically divided into logically divided into logical upper and lower sections of processing elements[each 8x8 subunit is divided into upper lower portions of subunits by switches in figures 6 and 7], and

wherein the processing elements in each of the sub-arrays are physically positioned so that the processing elements in the upper section are interleaved with the processing elements In the lower section (e.g., see figs. 2,6, and 10).

9. As per claim 43, the array of Hayashi provides switches for dividing the array in half to form logical sub-arrays and folding the logical sub-arrays and logically positioning the logical sub-arrays adjacent each other (e.g., see figs. 6 and 7). Further Hayashi taught (claim 44) the sub-arrays comprise switches for dividing the sub-arrays so that a portion of each logical sub-array is logically folded with a logical edge of the logical sub-array adjacent the dividing line. Hayashi also taught (claim 45) logically positioning the logical sub-arrays adjacent each other comprises logically positioning the sub arrays so that the folded portions of the sub-arrays face toward each other with the logical edges adjacent each other (e.g., see fig. 6 and 7). Here the facing of the toward each other does not provide any change in the operation of the system and the connections via the switches provide the same connections whether or not the folded portions are physically facing other sub-arrays.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (patent No. 5,689,661).

12. Hayashi taught the invention as substantially claimed including a data processing ("DP") system comprising: a logical array of processing elements logically arranged in a rectangular grid of logical rows and logical columns in which each processing element lies in only one logical row and one logical column (e.g., see fig. 6), the processing elements in the array being divided into four sub-arrays each including the processing elements in a respective quartile of the logical array (e.g., see col. 8, lines 57-col. 9, line 7)[four 8x8 subunits in the 16x16 array], each including processing elements in each of the sub-arrays being physically positioned in a folded arrangement in which the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical columns are physically interleaved with each other (e.g. see fig. 10 and col. 9, line 27-col. 10,line 8); and a system of conductors coupling the processing elements in each of the logical rows and columns of each other (e.g., see fig. 2,3a,3b,3c,3d,4a,4b,5a,5b,5c,6,8b,10).

13. As per claim 4, Hayashi taught a array or processing elements comprising 256 elements that is selectively divided into subunits (e.g., see fig. 6 and col. 8, line 57-col. 9, line7). One of ordinary skill would have been motivated to increase the size of the array to provide increased processing capability and throughput for processing increasingly demanding applications such as video applications. With this expansion one ordinary skill would have been motivated to expand the array in a regular fashion such as by a factor of 2 for easily addressing each processing element. This expansion

by 2 would have included an array of 32x32 comprising sub-arrays 16x16 or 256 processing elements.

14. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi as applied to claims 1 above, and further in view of Wilson (patent No. 6,728,862).

15. Wilson taught (claim 8) a plurality of registers logically positioned along one edge of a logical array at the end of respective logical rows (e.g. see col. 9, lines 41-54) and a plurality of column registers logically positioned along an adjacent edge of the logical array at the end of respective logical columns (e.g., see fig. 2 and col. 11, lines 6-67 and col. 10, lines 42-49).

16. As per claim 9, Wilson taught the logical array of processing elements comprises a upper edge and a logical lower edge and wherein the column registers are physically positioned so that they are physically adjacent processing elements adjacent lower edge (e.g., see fig. 2 and col. 11, lines 6-67 and col. 10, lines 42-49) but did not specifically detail column register were adjacent the logical upper edge. However Hayashi taught in figure 6 and 7 switches that have couplings to provide for connection from processors of the lower edge to processors of the upper edge. Therefore the combination of the Wilson registers along with the Hayashi coupling would have provided a physical positioning of the register to the upper edge of the array [the registers of Wilson are shown adjacent the lower registers however with connections from the lower edge to the upper edge the registers would be adjacent the upper edge].

17. As per claim 11, Wilson taught registers along a vertical edge and for same reasons described above for the upper registers the combination of the Wilson and Hayashi teachings would have provided registers adjacent the right and left edges.

18. As per claim 10,12 Since Wilson taught the scaling of the array with use of column for storing data transmitted register to/from the array one of ordinary skill would have been motivated to provide column registers between sub-arrays of an expanded array at least to more efficiently provide processing results (e.g., see col. 13, lines 1-13 of Wilson). This would have provided row registers in the middle of the of each sub-array with sub-array such as taught by Hayashi in figs 6 and 7).

19. It would have been obvious to one of ordinary skill in the DP art combine the teachings of Hayashi and Wilson. Both references were directed toward the problems of processing data using arrays of processing elements. The addition of the Wilson teaching of using row and column registers would have allowed the combined system to more efficiently processing large amounts of data as the timing of the processing could be controlled easier as the results data would be maintained in the registers.

20. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (patent No. 5,689,661) in view of Wilson (patent No. 6,728,862).

21. Hayashi taught the invention substantially as claimed including a data processing "DP") system comprising: coupling a plurality of processing elements to each other, the processing elements being logically arranged in a rectangular array of logical rows and columns that is divided into four logical sub-arrays each of which includes the

processing elements in a respective quartile logical array (e.g., see figs. 6 and 7). Hayashi taught an system of processing elements in respective locations so that the processing elements in different logical rows are physically interleaved with each other and the processing elements in different logical combinations are physically interleaved with each other and coupling the processing elements with each of the logical rows and columns to each other (e.g., see figs 3a, 3b, 3c, 3d, 4a, 5a, 5b, 5c, 6 and 7) [switches within array provide for interleaving of processing elements in rows and columns in a varied manner].

22. Hayashi did not expressly detail (claim 39) the fabrication of the system that was detailed in the Hayashi reference. However one of ordinary skill would have been motivated to fabricate (e.g., using integrated circuitry) the Hayashi system at least to take advantage of the processing throughput of the Hayashi system.

23. As per claims 40,41, in figure 6 Hayashi taught the system with connection between processing element of adjacent columns and in figs 3b and 4a taught connection between processors separated by three processors. In the implementation of the Hayashi system one of ordinary skill would have been motivated to fabricate the Hayashi system at least to provide the throughput of the Hayashi system.

24. As per claim 42 Wilson taught the logical array of processing elements comprises a upper edge and a logical lower edge and wherein the column registers are physically positioned so that they are physically adjacent processing elements adjacent lower edge (e.g., see fig. 2 and col. 11, lines 6-67 and col. 10, lines 42-49) but did not specifically detail column register were adjacent the logical upper edge. However

Hayashi taught in figure 6 and 7 switches that have couplings to provide for connection from processors of the lower edge to processors of the upper edge. Therefore the combination of the Wilson registers along with the Hayashi coupling would have provided a physical positioning of the register to the upper edge of the array [the registers of Wilson are shown adjacent the lower registers however with connections from the lower edge to the upper edge the registers would be adjacent the upper edge]. Wilson taught fabrication of the system (e.g., see col. 7, lines 1-20).

25. It would have been obvious to one of ordinary skill in the DP art combine the teachings of Hayashi and Wilson. Both references were directed toward the problems of processing data using arrays of processing elements. The addition of the Wilson teaching of using row and column registers would have allowed the combined system to more efficiently processing large amounts of data as the timing of the processing could be controlled easier as the results data would be maintained in the registers.

Allowable Subject Matter

Claims 13-38 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kean (patent No. 5,552,722) disclosed mask register for a configurable cellular array (e.g., see abstract).

Pechanek (patent No. 6,470,441) disclosed systems for manifold array processing (e.g., see abstract).

Barry (patent No. 6,769,056) disclosed system for manifold array processing (e.g., see abstract).

Birrittella et al. (patent No. 5,737,628) disclosed a multiprocessor computer system with interleaved processing element nodes (e.g., see abstract).

Dally (patent No. 6,598145) disclosed a system with an irregular netword of nodes (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER